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(FILE 'USPAT' ENTERED AT 16:05:59 ON 17 JAN 1999)
L1           310 S 395/287/CCLS
L2           372 S 395/280/CCLS
L3           662 S 395/309/CCLS
L4           197 S 395/285/CCLS
L5           271 S 395/306/CCLS
L6           165 S ISOCHRON? (P) CHANNEL
L7           548 S LINK? (10A) LIST (P) BUFFER?
L8             2 S L6 AND L7
L9             1 S L1 AND L6
L10            3 S L1 AND L7
L11            6 S L2 AND L7
L12            1 S L3 AND L6
L13            6 S L3 AND L7
L14            1 S L4 AND L7
L15            1 S L5 AND L7
L16         1748 S (TRANSMIT? OR RECEIV?) (P) SOFTWARE (P) ROUTINE
L17          175 S L16 AND CHANNEL (10A) IDENTIF?
L18           10 S L7 AND L1
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(FILE 'USPAT' ENTERED AT 16:05:59 ON 17 JAN 1999)
L1 310 S 395/287/CCLS
L2 372 S 395/280/CCLS
L3 662 S 395/309/CCLS
L4 197 S 395/285/CCLS
L5 271 S 395/306/CCLS
L6 165 S ISOCHRON? (P) CHANNEL
L7 548 S LINK? (10A) LIST (P) BUFFER?
L8 2 S L6 AND L7
L9 1 S L1 AND L6
L10 3 S L1 AND L7
L11 6 S L2 AND L7
L12 1 S L3 AND L6
L13 6 S L3 AND L7
L14 1 S L4 AND L7
L15 1 S L5 AND L7
L16 1748 S (TRANSMIT? OR RECEIV?) (P) SOFTWARE (P) ROUTINE
L17 175 S L16 AND CHANNEL (10A) IDENTIF?
L18 10 S L7 AND L17

=> d 18 1-

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US PAT NO: 5,754,789 [IMAGE AVAILABLE] L8: 1 of 2

SUMMARY:

BSUM(22)

These . . . being inserted when no other information is being transferred. The delay time in transmission is adjusted by a temporal alignment **buffer** in the channel modules to ensure that an integral multiple of packet transmission times are used for the total delay. . . arrival and start of each packet transmission. The four channel modules on a single interconnect controller chip share a common **buffer** pool with **linked list** entries for identifying which channel module is to propagate each received packet. The common **buffer** pool is segmented into sixteen (16) bit segments so that received packets may begin retransmission before completing arrival. This also. . .

DETDESC:

DETD(27)

When a channel module attempts to write received data into the packet **buffer** pool, the 12-bit address is simultaneously supplied to the routing table circuitry 29. The routing table circuitry outputs an 8-bit word that specifies which virtual channel may be used for the packet. This word is interpreted by the **buffer** control logic 41. The **buffer** control logic 41 maintains a **linked list** index to the registers of the packet **buffer** pool. Various registers may be free or occupied at different times irrespective of their actual location in the register file. The **linked list** index provides head-to-tail **linked list** pointers for all stored data packets and is used to index the packet **buffer** pool 40. By using the multi-ported register file that is accessible by all channels, each channel module may deposit received. . .

CLAIMS:

CLMS(1)

We . . .

communications channels and a plurality of adjacent nodes to each of which the node is coupled through a single communications **channel**, respectively, each of said nodes having an interconnect controller having means for controlling the exchange of data packets having a length of (W) bits over communications **channel**, wherein to transmit a packet having (W) bits plus (X) appended control bits requires a time (T), the method of. . .

packets stored in said common buffer pool of a node for transmission to an adjacent node through an appropriate communications **channel** where said selection of said appropriate communications **channel** is determined by indexing a destination id included in said data packet into a routing table;

assigning data packets in said routing table to **channel** modules having the fewest pending transactions;

extracting a data packet from said common buffer pool for transmission through said selected communications **channel**;

determining check code bits for said data packet based on the content of said data packet;

appending said data packet with said check code bits; and
continuously conveying data packets between adjacent nodes through **isochronous** coupled communications channels by conveying a data packet upon receiving a data packet.

CLAIMS:

CLMS(2)

2. . . .
data packets including packet age identification bits incremented to indicate the occurrence of certain conditions including delivery failure;
a plurality of **channel** modules each coupled to one of said plurality of communications ports, respectively, for controlling the flow of said data packets into and out of said interconnect controller wherein each of said **channel** modules may be coupled to a **channel** module of an adjacent node through interconnect controllers implemented in said adjacent nodes, said coupled **channel** modules of two adjacent nodes continuously exchanging a flow of data packets through an **isochronous** communications **channel**;
timing control logic means incorporated in each of said plurality of **channel** modules for adjusting the round trip delay (Dij) of packets exchanged between coupled adjacent **channel** modules to equal an integral number of T transmission times where Dij is the round trip time for a data. . . register having a variable depth which is set to adjust the round trip delay (Dij) for packets exchanged between adjacent **channel** modules to be an integral multiple of packet transmission time (T);
a clock means and means for synchronizing said clock means. . . interconnect controller with the clock means of said adjacent interconnect controller;
a common buffer pool coupled to said plurality of **channel** modules for buffering incoming and outgoing data packets; and
routing table logic in communication with said common buffer pool and said plurality of **channel** modules for routing data packets through appropriate **channel** modules.

CLAIMS:

CLMS(6)

6. . . .
packets are deleted if said packet age identification bits indicate packet age to be beyond a predetermined value;
a plurality of **channel** modules each coupled to one of said plurality of communications ports, respectively, for controlling the flow of said data packets into and out of said interconnect controller wherein each of said **channel** modules may be coupled to a **channel** module of an adjacent node through interconnect controllers implemented in said adjacent nodes, said coupled **channel** modules of two adjacent nodes continuously exchanging a flow of data packets through an **isochronous** communications **channel**;
timing control logic means incorporated in each of said plurality of **channel** modules for adjusting the round trip delay (Dij) of packets exchanged between coupled adjacent **channel** modules to equal an integral number of T transmission times where Dij is the round trip time for a data. . . a node i to a node j and back to node i;
a common buffer pool coupled to said plurality of **channel** modules for buffering incoming and outgoing data packets; and
routing table logic in communication with said common buffer pool and said plurality of **channel** modules for routing data packets through